200Gb/s QSFP56 SR4 Transceiver

APQP585ECDMS4A

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Product Features

- ✓ Four-channel full-duplex transceiver module
- ✓ Hot-pluggable QSFP28 footprint
- ✓ Supports 212.5Gb/s aggregate bit rate
- ✓ Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF
- ✓ 4x50Gb/s PAM4 VCSEL transmitter
- ✓ Single 3.3V power supply
- ✓ CMIS Rev4.0 compliant
- ✓ Complies with QSFP-DD MSA Rev 5.0 and IEEE 802.3bs/cd
- ✓ Complies with GR-468-CORE
- ✓ MPO-12 connector
- ✓ Power dissipation <5W (0~70°C)
- ✓ Operating case temperature range: 0 to 70°C

Applications

- ✓ 200GBASE-SR4 Ethernet

Product Selection

Part Number	Operating Case temperature	DDMI
APQP585ECDMS4A	Commercial(0~70℃)	Yes

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with EN 61000-4-3
- EMI compatible with FCC Part 15 Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 IEC 60950, IEC60825-1,2

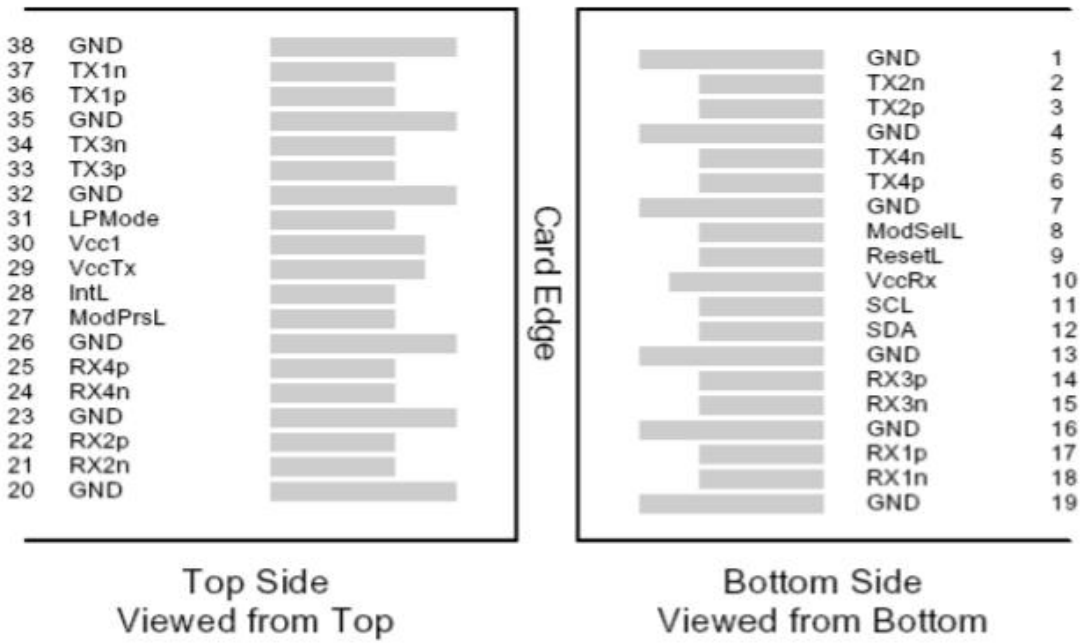
Pin Descriptions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3n	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3p	Transmitter Inverted Data Input	
35		GND	Ground	1

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.



Pin-out of Connector Block on Host Board

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.3		+3.6	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity(non-condensing)	RH	15		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.135		3.465	V	
Power Supply Current	Icc	-	-	1.44	A	Commercial
Case Operating Temperature	Tc	0	-	+70	°C	Commercial
Bit Rate Each Lane(PAM4)	Br		26.5625		Gbps	
Fiber Length: 2000 MHz·km 50/125μm MMF (OM3)				70	m	
Fiber Length: 4700 MHz·km 50/125μm MMF (OM4)				100	m	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Differential Input Impedance	Zin	90	100	110	Ω	
Differential Output Impedance	Zout	90	100	110		
Differential Input Voltage Amplitude	-	300	-	900	mVpp	1
Differential Output Voltage Amplitude	-	300	-	900	mVpp	
Bit Error Rate	BER		-	2.4E-4		2
Input Logic Level High	V_{IN}	2.0	-	Vcc	V	
Input Logic Level Low	V_{IL}	0		0.8	V	
Output Logic Level High	V_{ON}	Vcc-0.5	-	Vcc	V	
Output Logic Level Low	V_{OL}	0		0.4	V	

Notes:

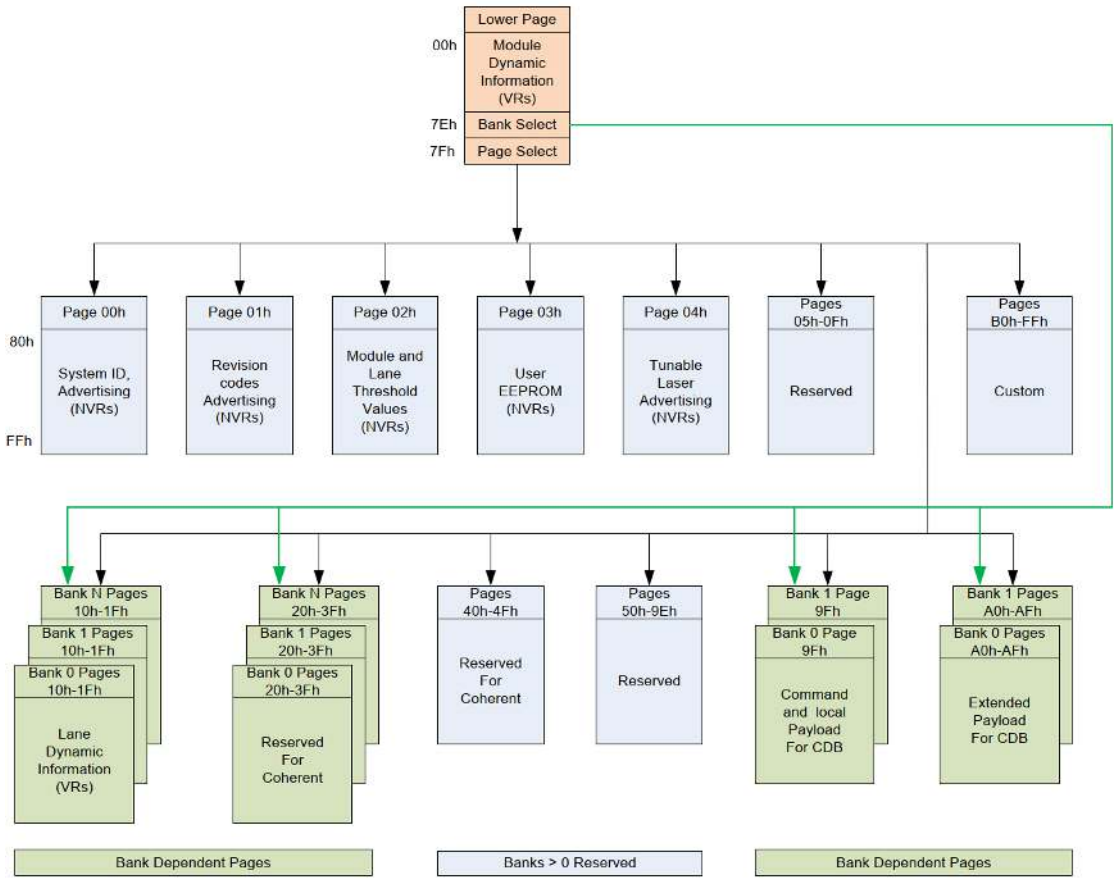
1. Suggested < 700mVpp input differential signal for better BER performance.
2. Compliant with 200GBASE-SR4 electrical specification in IEEE802.3cd standard.

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Center Wavelength	λ	840	850	860	nm	
RMS Spectral Width	Δ λ			0.6	nm	
Average launch power, each lane	Pout	-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane	OMA	-4.5		3	dBm	
Launch Power in OMA minus TDECQ		-5.9			dBm	
Transmitter and dispersion eye closure for PAM4(TDECQ), each lane	TDECQ			4.5	dB	
TDECQ – 10log10(Ceq), each lane				4.5	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction ratio	ER	3			dB	
Transmitter transition time, each lane				34	ps	
RINOMA				-128	dB/Hz	
Optical return loss tolerance				12	dB	
Encircled flux			86% at 19um 30% at 4.5nm			
Receiver						
Center wavelength, each lane	λ	840	850	860	nm	
Damage Threshold		5			dBm	
Average Receive Power (each lane)		-8.4		4	dBm	
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity (OMA_{outer}),each lane				Max(-6.5, SECQ-7.9)	dBm	
Stressed receiver sensitivity (OMA_{outer}), each lane				-3.4	dBm	
Stressed eye closure for PAM4 (SECQ), lane under test			4.5		dB	
SECQ – 10log10(Ceq) (max), lane under test			4.5		dB	
OMA_{outer} of each aggressor lane			3		dBm	

EEPROM Definitions

EEPROM complies with CMIS Rev4.0 .and EEPROM memory map specific data field description is as below:



Digital Diagnostic Monitoring Interface

Five transceiver parameter values are monitored. The following table defines the monitored parameter's accuracy.

Parameter	Related Bytes	Accuracy	Ref.
Case Temperature	14 to 15	±3°C	
Voltage	16 to 17	±5%	
Bias Current	Page 11h, Byte 170-177(2bytes each lane)	±10%	
TX Power(MPD)	Page 11h, Byte 154-161(2bytes each lane)	±3dB	1
RX Power	Page 11h, Byte 186-193(2bytes each lane)	±3dB	

Notes:

1. For Tx power monitoring, it is mandatory to use monitor-PD for sampling actual launch power.

Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Tang Rong	Xuming Di	DingZheng	New Released.	Aug 11, 2020

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